REMARKS

Claims 1-5, 7-12, 14-18 and 22-28 are currently pending in the application. Claims 6 and 13 have been canceled, claims 1 and 10 were amended, and claims 26-28 were added. Support for amended claims 1 and 10 can be found variously throughout the specification, for example, claims 6 and 13. No new matter has been added. Reconsideration of the rejected claims in view of the following remarks is respectfully requested.

Allowable Claims

Applicants appreciate the indication that claims 7-9 are allowed. Furthermore, Applicants submit that all of the claims are in condition for allowance for the following reasons.

35 U.S.C. §102 Rejections

Over Hachimine

Claims 1, 10, 12 and 15 were rejected under 35 U.S.C. §102(e) over US Patent No. 7,105,394 to HACHIMINE et al. This rejection is respectfully traversed.

In order to establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must disclose each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that a *prima facie* case of anticipation cannot be established because HACHIMINE fails to teach each and every element of the claims.

More particularly, independent claim 1 recites, *inter alia,*

> after the pFET stack is formed, providing a first layer of material at source/drain regions associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel; and
> after the nFET stack is formed, providing a second layer of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel.

Additionally, independent claim 10 recites, *inter alia,*

> forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel; and
> forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel

Applicants submit that HACHIMINE does not disclose or even suggest at least these features.

Applicants acknowledge that Fig. 37 of HACHIMINE shows a semiconductor device having nFETS and pFETS with first and second layers 24a and 24b which produce tensile and compressive stresses (see col. 28, lines 1-65). However, the Examiner has failed to point to any language in HACHIMINE which even remotely discloses or suggests that the first layer of material has a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel and/or that the second layer of material has a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel.

Furthermore, because Fig. 37 of HACHIMINE teaches to form the layers 24a and 24b over the surface of the structure and not within regions which are etched in the surface of the structure, HACHIMINE additionally fails to disclose or suggest that the

first layer of material is formed by placing a mask over the nFET stack, etching the regions of the pFET, and selectively growing the first layer of material within the regions of the pFET channel and/or that the second layer of material is formed by placing a mask over the pFET stack, etching regions of the nFET, and selectively growing the second layer of material within the regions of the nFET channel (claim 1). As such, HACHIMINE also fails to teach etching regions of the pFET structure and the nFET structure covered by a protective layer and after the pFET stack is formed and the pFET structure is covered by the protective layer, masking the nFET structure and forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel and/or after the nFET stack is formed and the nFET structure is covered by the protective layer, masking the pFET structure and forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel (claim 10).

Thus, Applicants respectfully submit that independent claims 1 and 10, and claims 12 and 15, which depend from claim 10 are allowable.

Accordingly, Applicants respectfully request that the above-noted rejection under 35 U.S.C. § 102(e) should be withdrawn.

Over Hoffman

Claims 10, 12 and 15 were rejected under 35 U.S.C. §102(e) over US Patent Application Publication No. 2004/0253776 to HOFFMANN et al. This rejection is respectfully traversed.

In order to establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must disclose each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that a *prima facie* case of anticipation cannot be established because HOFFMANN fails to teach each and every element of the claims.

Again, independent claim 10 recites, *inter alia,*

> forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel; and
> forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel

Applicants submit that HOFFMANN does not disclose or even suggest at least these features.

Applicants acknowledge that Fig. 2 of HOFFMANN shows a semiconductor device having nFETS and pFETS with first and second layers 213 and 214 which produce stresses (see paragraphs [0021] – [0023]). However, the Examiner has failed to point to any language in HACHIMINE which even remotely discloses or suggests that the first layer of material has a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel and/or that the second layer of material has a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel.

Nor can the Examiner do so because HOFFMAN is concerned with the lattice spacing difference between the layers 213 and 214 and the electrodes 130 and not between the layers 213 and 214 and the substrate. Indeed, paragraph [0021]

specifically states that "layer 214 has a lattice spacing different than NMOS gate electrode 130 and PMOS gate electrode 132" and that "layer 213 has a lattice spacing greater than NMOS gate electrode 130."

Furthermore, because Fig. 2 of HOFFMANN teaches to form the layers 213 and 214 over the stack 130 and not within regions which are etched in the surface of the structure, HOFFMANN additionally fails to disclose or suggest etching regions of the pFET structure and the nFET structure covered by a protective layer and after the pFET stack is formed and the pFET structure is covered by the protective layer, masking the nFET structure and forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel and/or after the nFET stack is formed and the nFET structure is covered by the protective layer, masking the pFET structure and forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel (claim 10).

Thus, Applicants respectfully submit that independent claim 10, and claims 12 and 15, which depend from claim 10 are allowable.

Accordingly, Applicants respectfully request that the above-noted rejection under 35 U.S.C. § 102(e) should be withdrawn.

35 U.S.C. §103 Rejections

Over Hoffmann alone

Claim 16 was rejected under 35 U.S.C. §103(a) over HOFFMANN alone. This

rejection is respectfully traversed.

As stated previously, Applicants submit that this basis of rejection is improper at least because HOFFMAN fails to disclose or suggest that the first layer of material has a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel and/or that the second layer of material has a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel (claim 10).

Nor can the Examiner argue to the contrary because HOFFMAN is concerned with the lattice spacing difference between the layers 213 and 214 and the electrodes 130 and not between the layers 213 and 214 and the substrate. Indeed, paragraph [0021] specifically states that "layer 214 has a lattice spacing different than NMOS gate electrode 130 and PMOS gate electrode 132" and that "layer 213 has a lattice spacing greater than NMOS gate electrode 130."

Furthermore, because Fig. 2 of HOFFMANN teaches to form the layers 213 and 214 over the stack 130 and not within regions which are etched in the surface of the structure, HOFFMANN additionally fails to disclose or suggest etching regions of the pFET structure and the nFET structure covered by a protective layer and after the pFET stack is formed and the pFET structure is covered by the protective layer, masking the nFET structure and forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel and/or after the nFET stack is formed and the nFET structure is covered by the protective layer, masking the pFET structure and forming a second material with a lattice constant different than the base lattice constant

of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel (claim 10).

Accordingly, Applicants respectfully request that the above-noted §103(a) rejection of claim 16, which depends from claim 10, be withdrawn.

Over Hoffmann with Yeo

Claims 10-12, 17 and 22-25 were rejected under 35 U.S.C. §103(a) over HOFFMANN in view of US Patent No. 6,921,913 (incorrectly designated as 6,923,913) to YEO et al. This rejection is respectfully traversed.

The Examiner acknowledges that HOFFMANN fails to disclose, among other things, the recited materials for the first and second layers. However, the Examiner explains that such features are taught by YEO and that it would have been obvious to combine the teachings of these documents. Applicants respectfully submit that a *prima facie* case of obviousness has not been established as the applied references fail to teach each and every element of the claims.

Again, independent claim 10 recites, *inter alia,*

> forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel; and
> forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel

Additionally, independent claim 22 recites, *inter alia,*

> forming channels in the substrate about the pFET stack;
> growing a layer of material in the channels associated with the pFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a compressive state within the channels of the pFET stack;

forming channels in the substrate about the nFET stack; and
growing a layer of material in the channels associated with the nFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a tensile state within the channels of the nFET stack.

With regard to claim 10, Applicants submit that this basis of rejection is improper at least HOFFMAN fails to disclose or suggest that the first layer of material has a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel and/or that the second layer of material has a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel (claim 10). Nor can the Examiner argue to the contrary because HOFFMAN is concerned with the lattice spacing difference between the layers 213 and 214 and the electrodes 130 and not between the layers 213 and 214 and the substrate. Indeed, paragraph [0021] specifically states that "layer 214 has a lattice spacing different than NMOS gate electrode 130 and PMOS gate electrode 132" and that "layer 213 has a lattice spacing greater than NMOS gate electrode 130."

Furthermore, because Fig. 2 of HOFFMANN teaches to form the layers 213 and 214 over the stack 130 and not within regions which are etched in the surface of the structure, HOFFMANN additionally fails to disclose or suggest etching regions of the pFET structure and the nFET structure covered by a protective layer and after the pFET stack is formed and the pFET structure is covered by the protective layer, masking the nFET structure and forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel and/or after the nFET stack is formed and the nFET structure is covered by the protective layer, masking the pFET structure and

forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel (claim 10).

YEO does not cure the deficiencies of HOFFMANN regarding claim 10. While it is true that YEO describes various embodiments which utilize lattice-mismatched zones in regions of the nFET and pFET, YEO does not disclose the recited protective layer and specifically fails to disclose or suggest etching regions of the pFET structure and the nFET structure covered by a protective layer and after the pFET stack is formed and the pFET structure is covered by the protective layer, masking the nFET structure and forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel and/or after the nFET stack is formed and the nFET structure is covered by the protective layer, masking the pFET structure and forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel (claim 10).

With regard to claim 22, Applicants submit that this basis of rejection is improper at least because HOFFMAN fails to disclose or suggest forming channels in the substrate about the pFET stack, much less, growing a layer of material in the channels associated with the pFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a compressive state within the channels of the pFET stack and/or forming channels in the substrate about the nFET stack, much less, growing a layer of material in the channels associated with the nFET stack, wherein after the growing, the

layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a tensile state within the channels of the nFET stack (claim 22). Again, HOFFMAN is concerned with the lattice spacing difference between the layers 213 and 214 and the electrodes 130 and not between the layers 213 and 214 and the substrate. Indeed, paragraph [0021] specifically states that "layer 214 has a lattice spacing different than NMOS gate electrode 130 and PMOS gate electrode 132" and that "layer 213 has a lattice spacing greater than NMOS gate electrode 130."

Furthermore, because Fig. 2 of HOFFMANN teaches to form the layers 213 and 214 over the stack 130 and not within regions which are etched in the surface of the structure, HOFFMANN clearly fails to disclose or suggest forming channels in the substrate about the pFET stack, much less, growing a layer of material in the channels associated with the pFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a compressive state within the channels of the pFET stack and/or forming channels in the substrate about the nFET stack, much less, growing a layer of material in the channels associated with the nFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a tensile state within the channels of the nFET stack (claim 22).

YEO does not cure the deficiencies of HOFFMANN regarding claim 22. While it is true that YEO describes various embodiments which utilize lattice-mismatched zones in regions of the nFET and pFET, YEO does not disclose growing a layer of material in

the channels associated with the pFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a compressive state within the channels of the pFET stack and/or growing a layer of material in the channels associated with the nFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a tensile state within the channels of the nFET stack (claim 22). Indeed, the fact that YEO teaches to use lattice-mismatched zones is contrary to utilizing a lattice structure that tends to match a lattice structure of an underlying portion of the substrate.

Accordingly, Applicants submit that no proper combination of HOFFMANN and YEO discloses or suggests the combination of features recited in at least claims 10 and 22.

Moreover, in addition to failing to disclose the combination of features recited in the above-noted claims 10 and 22, Applicants submit no proper combination of these documents discloses or suggests the combination of features recited in dependent claims 11, 12, 17 and 23-25, which also respectfully contain all of the features of claims 10 and 22.

Accordingly, Applicants respectfully submit that the above-noted rejection under 35 U.S.C. § 103(a) should be withdrawn.

Over Yeo alone

Claims 1-5, 10-12, 14-18 and 22-25 (while not listed in the preamble of the rejection, claim 10 is assumed to be rejected because it was discussed in the body of

the rejection) were rejected under 35 U.S.C. §103(a) over YEO alone. The rejection is respectfully traversed.

The Examiner asserts that YEO discloses or suggests all of the features recited in the above-noted claims. Furthermore, the Examiner apparently believes that any missing features are obvious. Applicants respectfully submit that a *prima facie* case of obviousness has not been established as the applied references fail to teach each and every element of the claims.

Independent claim 1 recites, *inter alia,*

> wherein the first layer of material is formed by placing a mask over the nFET stack, etching the regions of the pFET, and selectively growing the first layer of material within the regions of the pFET channel; and
> wherein the second layer of material is formed by placing a mask over the pFET stack, etching regions of the nFET, and selectively growing the second layer of material within the regions of the nFET channel.

Additionally, independent claim 10 recites, *inter alia,*

> etching regions of the pFET structure and the nFET structure covered by a protective layer;
> after the pFET stack is formed and the pFET structure is covered by the protective layer, masking the nFET structure and forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel;
> after the nFET stack is formed and the nFET structure is covered by the protective layer, masking the pFET structure and forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel.

Finally, independent claim 22 recites, *inter alia,*

> forming channels in the substrate about the pFET stack;
> growing a layer of material in the channels associated with the pFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a compressive state within the channels of the pFET stack;
> forming channels in the substrate about the nFET stack; and

growing a layer of material in the channels associated with the nFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a tensile state within the channels of the nFET stack.

With regard to claim 1, Applicants note that while it is true that YEO describes various embodiments which utilize lattice-mismatched zones in regions of the nFET and pFET, YEO does not disclose or suggest that the first layer of material is formed by placing a mask over the nFET stack, etching the regions of the pFET, and selectively growing the first layer of material within the regions of the pFET channel and that the second layer of material is formed by placing a mask over the pFET stack, etching regions of the nFET, and selectively growing the second layer of material within the regions of the nFET channel (claim 1). Indeed, the Examiner has acknowledged as much on page 8 of the instant Office action.

With regard to claim 10, Applicants submit that YEO does not disclose the recited protective layer and specifically fails to disclose or suggest etching regions of the pFET structure and the nFET structure covered by a protective layer and after the pFET stack is formed and the pFET structure is covered by the protective layer, masking the nFET structure and forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel and/or after the nFET stack is formed and the nFET structure is covered by the protective layer, masking the pFET structure and forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel (claim 10).

With regard to claim 22, Applicants submit that YEO does not disclose growing a layer of material in the channels associated with the pFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a compressive state within the channels of the pFET stack and/or growing a layer of material in the channels associated with the nFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a tensile state within the channels of the nFET stack (claim 22). As explained above, the fact that YEO teaches to use lattice-mismatched zones is contrary to utilizing a lattice structure that tends to match a lattice structure of an underlying portion of the substrate.

Accordingly, Applicants submit that no proper modification of YEO discloses or suggests the combination of features recited in at least claims 1, 10 and 22.

Moreover, in addition to failing to disclose the combination of features recited in the above-noted claims 1, 10 and 22, Applicants submit no proper combination of these documents discloses or suggests the combination of features recited in dependent claims 2-5, 11, 12, 14-18 and 23-25, which also respectfully contain all of the features of claims 1, 10 and 22.

Accordingly, Applicants respectfully submit that the above-noted rejection under 35 U.S.C. § 103(a) should be withdrawn.

Over Yeo with Park

Claims 6 and 13 were rejected under 35 U.S.C. §103(a) over YEO in view of US

Patent Application Publication No. 2003/0022460 to PARK (incorrectly designated as PARKS). This rejection is respectfully traversed.

The Examiner acknowledges that YEO fails to disclose, among other things, the recited masking, etching, and growing steps. However, the Examiner explains that such features are taught by PARK and that it would have been obvious to combine the teachings of these documents. Applicants respectfully submit that a *prima facie* case of obviousness has not been established as the applied references fail to teach each and every element of the claims.

Again, independent claim 1 recites, *inter alia,*

> wherein the first layer of material is formed by placing a mask over the nFET stack, etching the regions of the pFET, and selectively growing the first layer of material within the regions of the pFET channel; and
> wherein the second layer of material is formed by placing a mask over the pFET stack, etching regions of the nFET, and selectively growing the second layer of material within the regions of the nFET channel.

Additionally, independent claim 10 recites, *inter alia,*

> etching regions of the pFET structure and the nFET structure covered by a protective layer;
> after the pFET stack is formed and the pFET structure is covered by the protective layer, masking the nFET structure and forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel;
> after the nFET stack is formed and the nFET structure is covered by the protective layer, masking the pFET structure and forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel.

With regard to claim 1, Applicants again note that while it is true that YEO describes various embodiments which utilize lattice-mismatched zones in regions of the nFET and pFET, YEO does not disclose or suggest that the first layer of material is

formed by placing a mask over the nFET stack, etching the regions of the pFET, and selectively growing the first layer of material within the regions of the pFET channel and that the second layer of material is formed by placing a mask over the pFET stack, etching regions of the nFET, and selectively growing the second layer of material within the regions of the nFET channel (claim 1). Indeed, the Examiner has acknowledged as much on page 8 of the instant Office action.

PARK, however, does not cure the deficiencies of YEO. While it is true that PARK teaches to use an ARL layer 208 in the device of Fig. 5C, the layer 208 is clearly not utilized as a mask over the nFET stack and/or as a mask over the pFET stack as recited claim 1. Accordingly, there is no basis for modifying YEO in view of PARK and even if there were, such a combination of teachings would not disclose or suggest the combination of features recited in claim 1.

With regard to claim 10, Applicants submit that YEO does not disclose the recited protective layer and specifically fails to disclose or suggest etching regions of the pFET structure and the nFET structure covered by a protective layer and after the pFET stack is formed and the pFET structure is covered by the protective layer, masking the nFET structure and forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel and/or after the nFET stack is formed and the nFET structure is covered by the protective layer, masking the pFET structure and forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel (claim 10).

Again, PARK does not cure the deficiencies of YEO. While it is true that PARK teaches to use an ARL layer 208 in the device of Fig. 5C, the layer 208 is clearly not utilized as a mask to mask the nFET structure and/or to mask the pFET structure as recited claim 10. Accordingly, there is no basis for modifying YEO in view of PARK and even if there were, such a combination of teachings would not disclose or suggest the combination of features recited in claim 10.

Accordingly, Applicants submit that no proper combination of YEO and PARK discloses or suggests the combination of features recited in at least claims 1 and 10.

Moreover, in addition to failing to disclose the combination of features recited in the above-noted claims 1 and 10, Applicants submit that the instant rejection of claims 6 and 13 is moot inasmuch as these claims have been canceled.

Accordingly, Applicants respectfully submit that the above-noted rejection under 35 U.S.C. § 103(a) should be withdrawn.

New Claims are also Allowable

Applicants submit that the new claims 26-28 are allowable over the applied art of record. Specifically, claims 26-28 depend from claims 1 and 10 which are believed to be allowable. Additionally, claims 26-28 recite a combination of features which are clearly not disclosed or suggested by the applied art of record. Accordingly, Applicants respectfully request consideration of these claims and further request that the above-noted claims be indicated as being allowable.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0458.

Respectfully submitted,
Haujie CHEN, *et al.*

Andrew M. Calderon
Reg. No. 38,093

April 24, 2007
GREENBLUM & BERNSTEIN, P.L.C.
1950 Roland Clarke Place
Reston, VA 20191
(703) 716-1191